

IN THE CLAIMS

1. (Currently Amended) A computerized method comprising:
 - identifying a first stream of data stored in first source register and a second stream of data stored in a second source register; and
 - performing a single bit-level interleaving instruction on the first stream of data and the second stream of data to generate a combined stream of data in a destination register,
wherein syntax of the bit-level interleaving instruction is expressed as

Dest = Bit_interleaver(Src₁, Src₂),

wherein Dest identifies the destination register, Src₁ identifies the first source register, Src₂ identifies the second source register, and Bit_interleaver identifies a bit interleaving operation.

2. (Previously Presented) The method of claim 1 further comprising:
 - receiving the interleaving instruction.
3. Canceled.
4. Canceled.
5. (Original) The method of claim 1 wherein each of the first stream and the second stream includes 16 bits of encoded data.
6. (Currently Amended) An apparatus comprising:
 - an instruction memory to store an interleaving instruction;

an instruction sequencer, coupled to the instruction memory, to receive the interleaving instruction;

an execution unit, coupled to the instruction sequencer, to execute the interleaving instruction, the interleaving instruction generating a combined stream of data by a bit-level interleaving of a first stream of data and a second stream of data; and

a register file, coupled to the execution unit, the register file including a first source register to hold the first stream of data, a second source register to hold the second stream of data, and a destination register to hold the combined stream of data, wherein syntax of the interleaving instruction is expressed as

$$\underline{Dest = Bit_interleaver(Src_1, Src_2)},$$

wherein Dest identifies the destination register, Src₁ identifies the first source register, Src₂ identifies the second source register, and Bit_interleaver identifies a bit interleaving operation.

7. (Canceled)
8. (Original) The apparatus of claim 6 wherein each of the first stream and the second stream includes 16 bits of encoded data.
9. (Currently Amended) A computer system comprising:
 - a memory to store computer data and instructions; and
 - a processor, coupled to the memory, to receive a first stream of data, a second stream of data, and an interleaving instruction from the memory, to store the first stream of data in a first source register and a second stream of data in a second source register, and to execute

the interleaving instruction on the first stream of data and the second stream of data, the interleaving instruction to generate a combined stream of data in a destination register by a bit-level interleaving of the first stream of data and the second stream of data, wherein syntax of the interleaving instruction is expressed as

$Dest = Bit_interleaver(Src_1, Src_2)$,

wherein $Dest$ identifies the destination register, Src_1 identifies the first source register, Src_2 identifies the second source register, and $Bit_interleaver$ identifies a bit interleaving operation.

10. Canceled.

11. (Canceled)

12. (Original) The system of claim 9 wherein each of the first stream and the second stream includes 16 bits of encoded data.

13. (Currently Amended) A computer readable medium that provides instructions, which when executed on a processor, cause said processor to perform operations comprising:

identifying a first stream of data stored in a first source register and a second stream of data stored in a second source register; and

performing a single bit-level interleaving instruction on the first stream of data and the second stream of data to generate a combined stream of data in a destination register, wherein syntax of the bit-level interleaving instruction is expressed as

$Dest = Bit_interleaver(Src_1, Src_2)$,

wherein *Dest* identifies the destination register, *Src₁* identifies the first source register, *Src₂* identifies the second source register, and *Bit interleaver* identifies a bit interleaving operation.

14. (Previously Presented) The computer readable medium of claim 13 providing further instructions causing the processor to perform operations comprising:
receiving the interleaving instruction.

15. (Canceled).

16. (Canceled)

17. (Original) The computer readable medium of claim 13 wherein each of the first stream and the second stream includes 16 bits of encoded data.

18. (Original) The method of claim 1 wherein the bit interleaving instruction is a single executed instruction.

19. Canceled.